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# Menu

- SPI Concepts
  - >Problems in serial communications
    - – Timing Synchronization: How do you line up the bit boundaries?
    - – Message Synchronization: How do you line up messages?
  - >Synchronous data solves first problem by sending clock along with message
    - – SPI performs a "physical-level" form of serial communication
  - >Section 11.4 in the S&HE Book Covers the SPI system


See docs/examples on web-site:
**doc8331 (Sec 22), doc2595,**
**GCPU++: SPI_*.asm, LSM6DSL**
**In demo video** (but **NOT on website**): spi_m_swap_byte.asm, spi_s_swap_byte.asm, spi_m_s_swap_byte.asm, spi_m_swap_bytes.asm, spi_s_swap_bytes.asm



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# What is SPI?

- SPI = Serial Peripheral Interface
  - >Established by Motorola
- Synchronous serial data link operating in full duplex mode
  - >Signals are carried in both directions on separate wires
- Communicate with many devices, including non-SPI devices
- SPI devices can be either a **Master** or a **Student**

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## Master/Student


- The Karate Kid
  - > Old movie (~1984)
- Cobra Kai
  - > YouTube/Netflix
    - – Season 5 now available

https://youtu.be/3PycZtfns_U
https://youtu.be/Bg21M2zwG9Q




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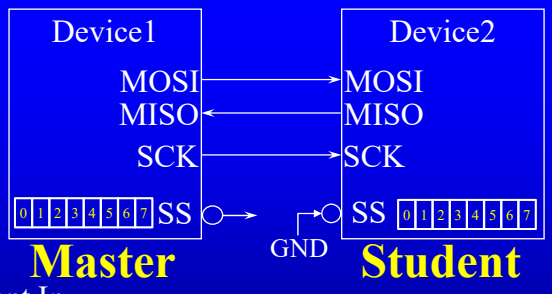
## Simple SPI Setup

- 4 Interface Signals
  - >**SCK** - Serial Clock
    - – Output for master
    - – Input for student
  - >**SS**(L) - Student Select
    - – Input for student
    - – Unrelated output for master
  - >**MOSI** - Master Out/Student In
  - >**MISO** - Master In/Student Out
- May use 3 or 4 pins




| | Master SPI Data Register | Student SPI Data Register |
|---|---|---|
| Initial | XXXX XXXX | YYYY YYYY |
| After 8 SCK's | YYYY YYYY | XXXX XXXX |

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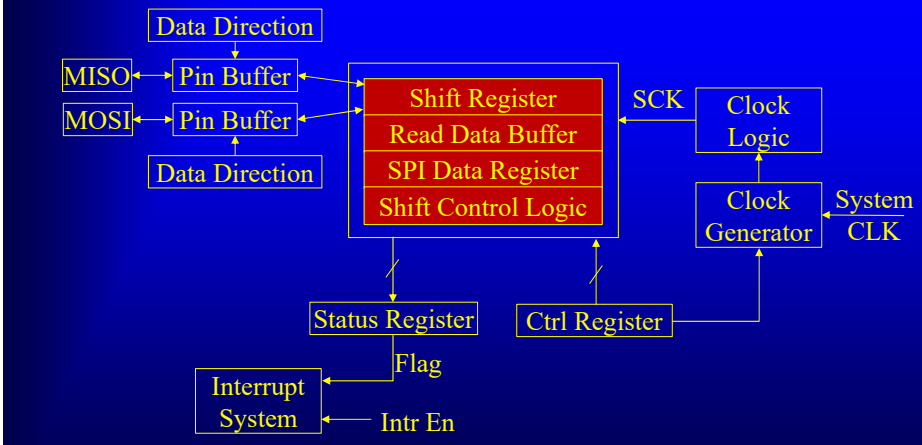
## Simple SPI Block Diagram

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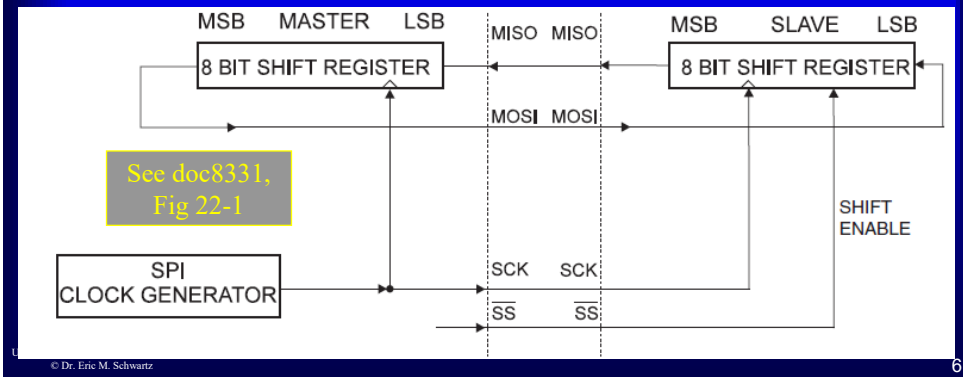
## XMEGA SPI

- System consists of two shift registers and a master clock generator
- Data is **shifted out** the master's MISO pin
- Data is **shifted in** the master's MOSI pin

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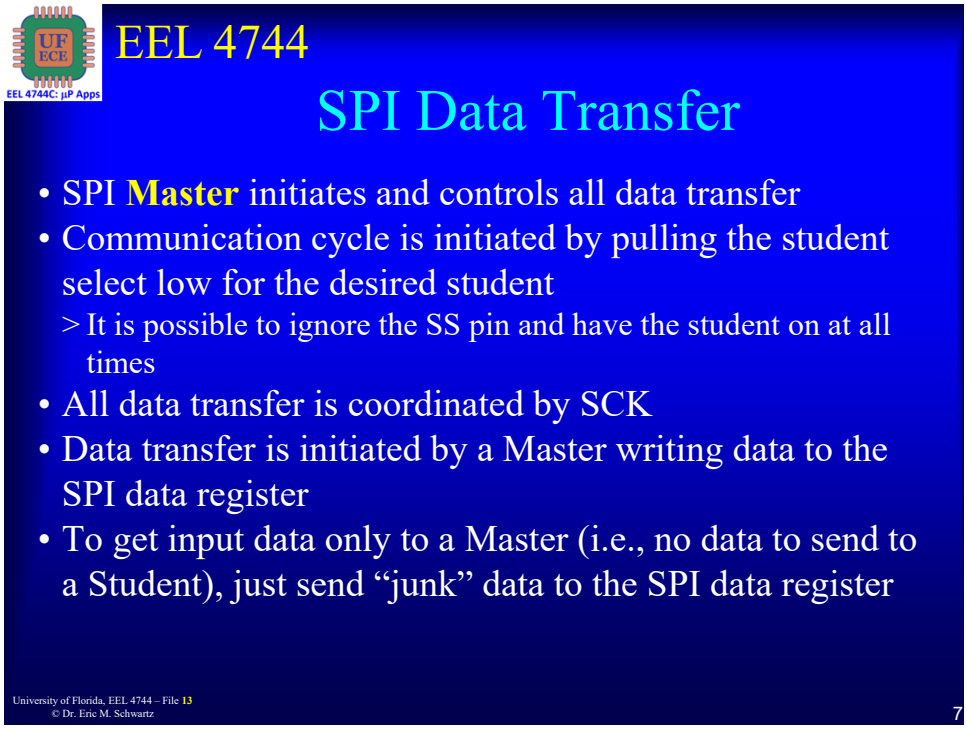
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SPI Data Transfer
• SPI Master initiates and controls all data transfer
• Communication cycle is initiated by pulling the student select low for the desired student
> It is possible to ignore the SS pin and have the student on at all times
• All data transfer is coordinated by SCK
• Data transfer is initiated by a Master writing data to the SPI data register
• To get input data only to a Master (i.e., no data to send to a Student), just send "junk" data to the SPI data register
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SPI Details
• Message Length: 8-bits
• For many SPI systems, the shift register can be in either direction, MSB to LSB or LSB to MSB
> For XMEGA, direction is determined by DORD in the SPI CTRL register
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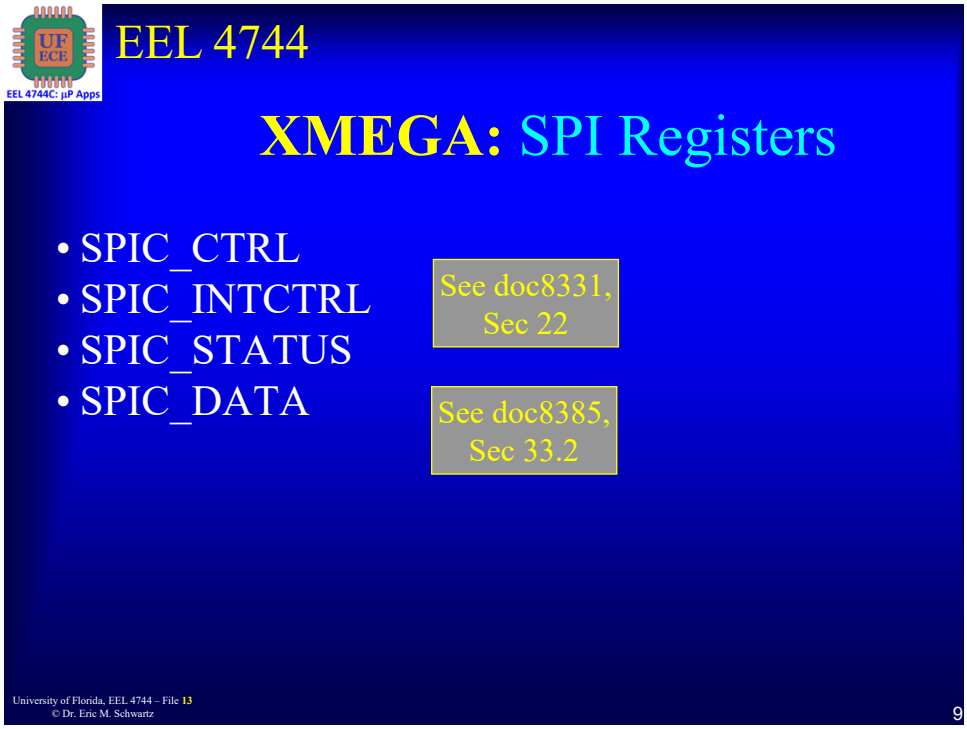
EEL 4744
EEL 4744C: µP Apps
XMEGA: SPI Registers
• SPIC_CTRL
• SPIC_INTCTRL
• SPIC_STATUS
• SPIC_DATA
See doc8331, Sec 22
See doc8385, Sec 33.2
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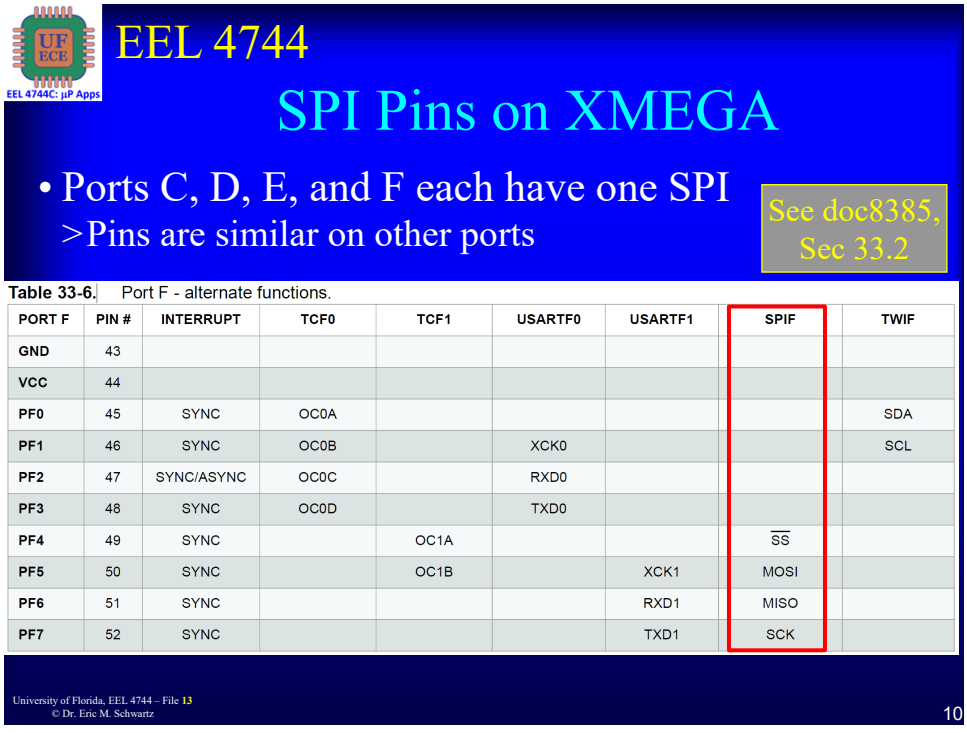
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EEL 4744C: µP Apps
SPI Pins on XMEGA
• Ports C, D, E, and F each have one SPI
>Pins are similar on other ports
See doc8385, Sec 33.2
Table 33-6. Port F - alternate functions.
PORT F | PIN # | INTERRUPT | TCF0 | TCF1 | USARTF0 | USARTF1 | SPIF | TWIF
GND | 43
VCC | 44
PF0 | 45 | SYNC | OC0A | SDA
PF1 | 46 | SYNC | OC0B | XCK0 | SCL
PF2 | 47 | SYNC/ASYNC | OC0C | RXD0
PF3 | 48 | SYNC | OC0D | TXD0
PF4 | 49 | SYNC | OC1A | SS
PF5 | 50 | SYNC | OC1B | XCK1 | MOSI
PF6 | 51 | SYNC | RXD1 | MISO
PF7 | 52 | SYNC | TXD1 | SCK
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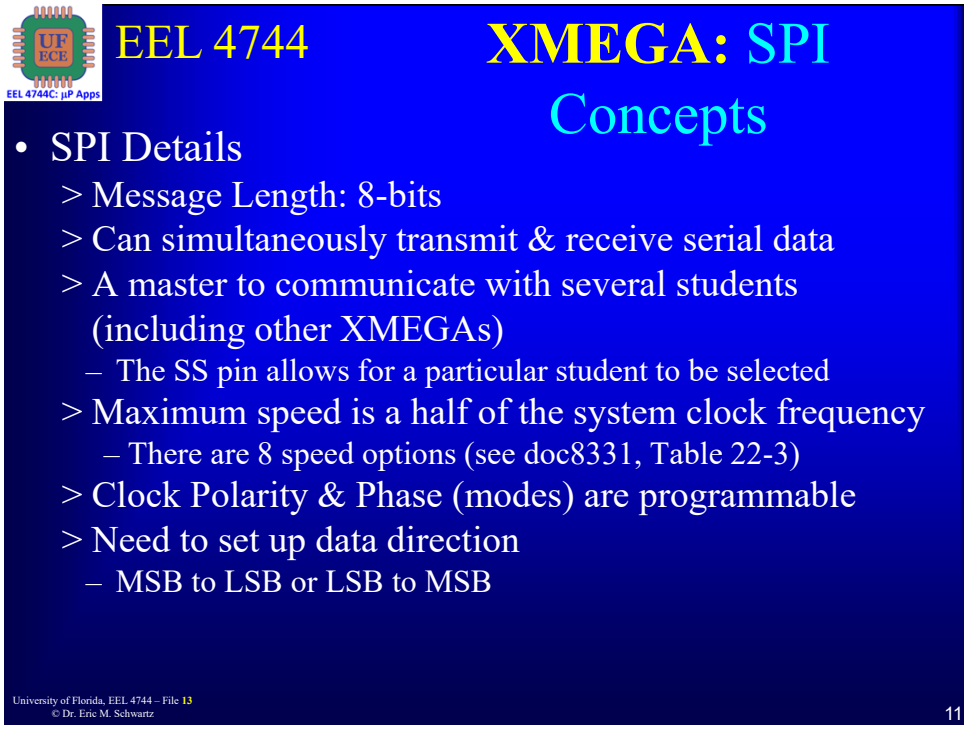
EEL 4744
XMEGA: SPI Concepts
• SPI Details
> Message Length: 8-bits
> Can simultaneously transmit & receive serial data
> A master to communicate with several students (including other XMEGAs)
– The SS pin allows for a particular student to be selected
> Maximum speed is a half of the system clock frequency
– There are 8 speed options (see doc8331, Table 22-3)
> Clock Polarity & Phase (modes) are programmable
> Need to set up data direction
– MSB to LSB or LSB to MSB
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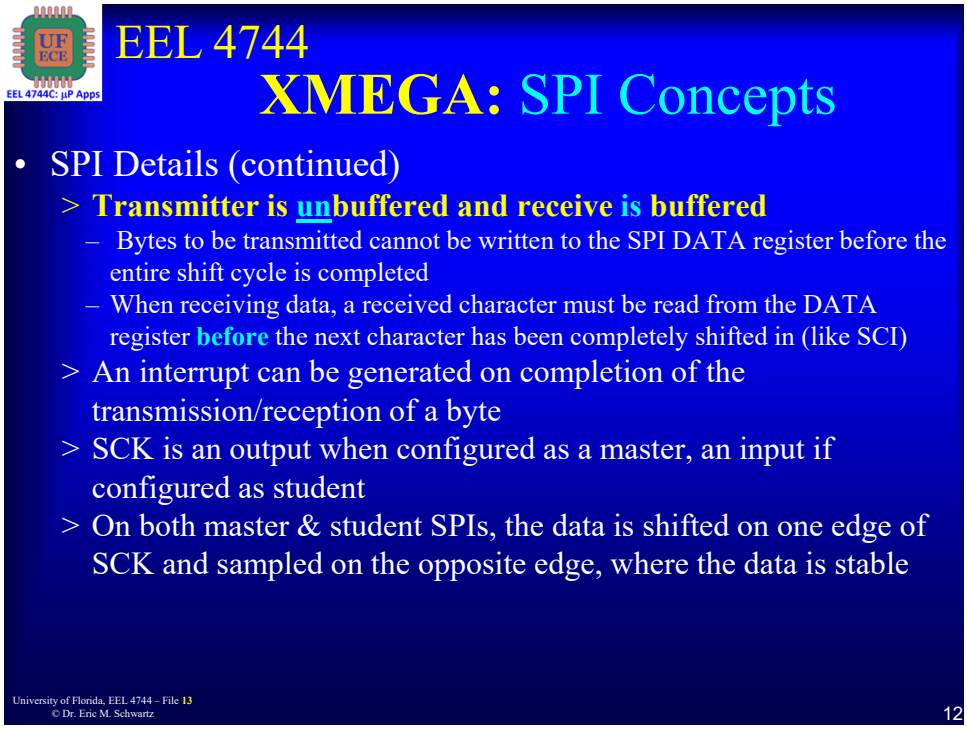
EEL 4744
XMEGA: SPI Concepts
• SPI Details (continued)
> Transmitter is unbuffered and receive is buffered
– Bytes to be transmitted cannot be written to the SPI DATA register before the entire shift cycle is completed
– When receiving data, a received character must be read from the DATA register before the next character has been completely shifted in (like SCI)
> An interrupt can be generated on completion of the transmission/reception of a byte
> SCK is an output when configured as a master, an input if configured as student
> On both master & student SPIs, the data is shifted on one edge of SCK and sampled on the opposite edge, where the data is stable
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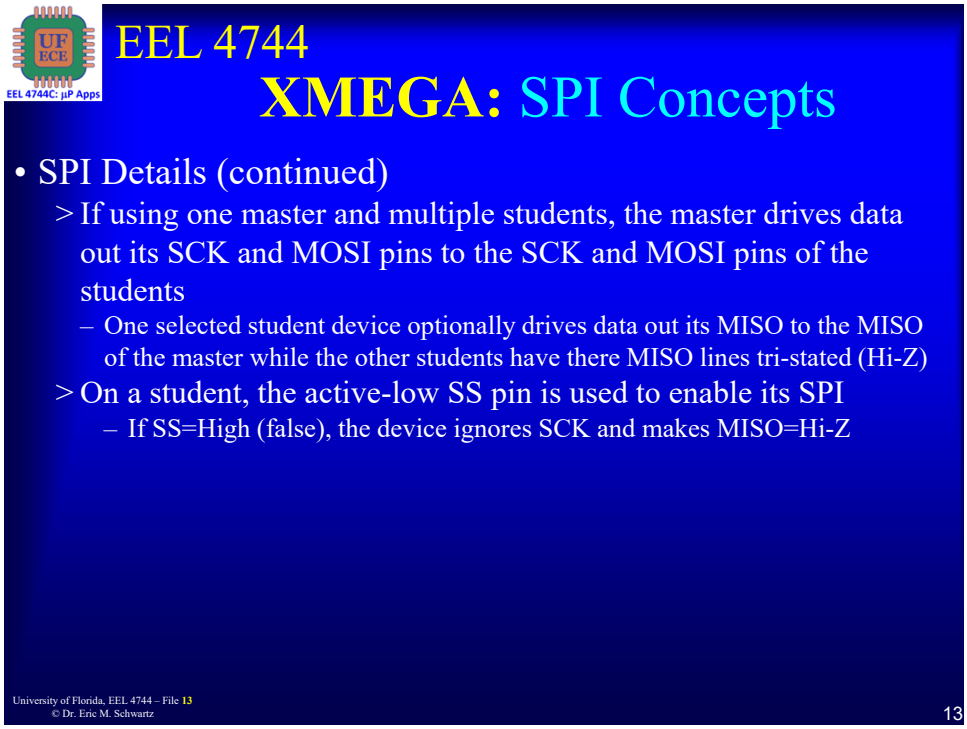
EEL 4744
XMEGA: SPI Concepts
• SPI Details (continued)
> If using one master and multiple students, the master drives data out its SCK and MOSI pins to the SCK and MOSI pins of the students
– One selected student device optionally drives data out its MISO to the MISO of the master while the other students have there MISO lines tri-stated (Hi-Z)
> On a student, the active-low SS pin is used to enable its SPI
– If SS=High (false), the device ignores SCK and makes MISO=Hi-Z
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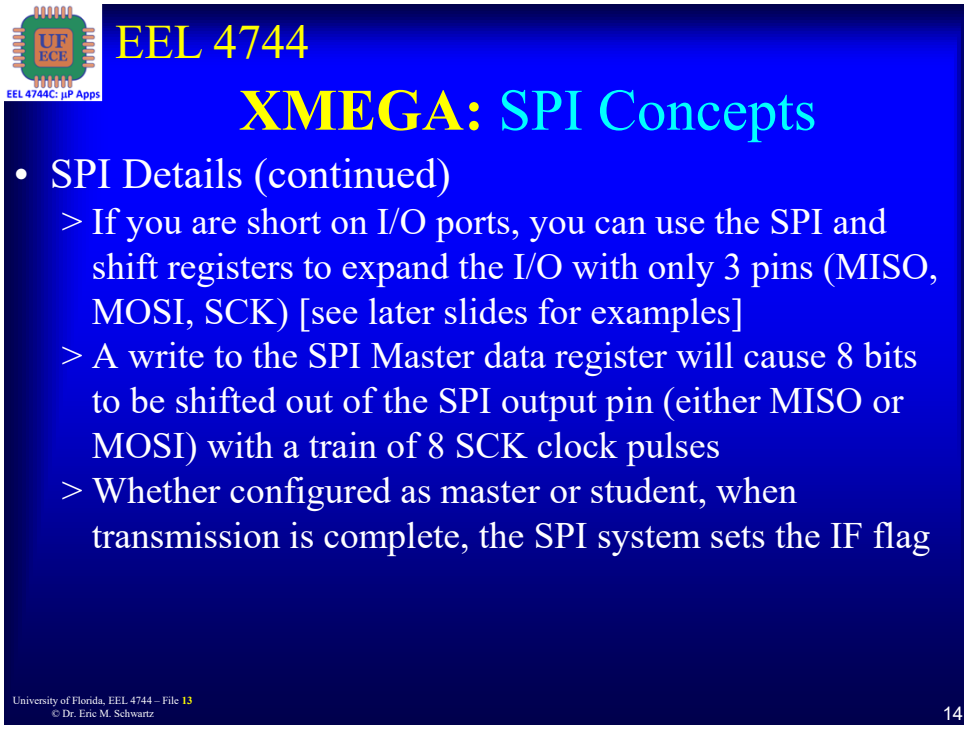
EEL 4744
XMEGA: SPI Concepts
• SPI Details (continued)
> If you are short on I/O ports, you can use the SPI and shift registers to expand the I/O with only 3 pins (MISO, MOSI, SCK) [see later slides for examples]
> A write to the SPI Master data register will cause 8 bits to be shifted out of the SPI output pin (either MISO or MOSI) with a train of 8 SCK clock pulses
> Whether configured as master or student, when transmission is complete, the SPI system sets the IF flag
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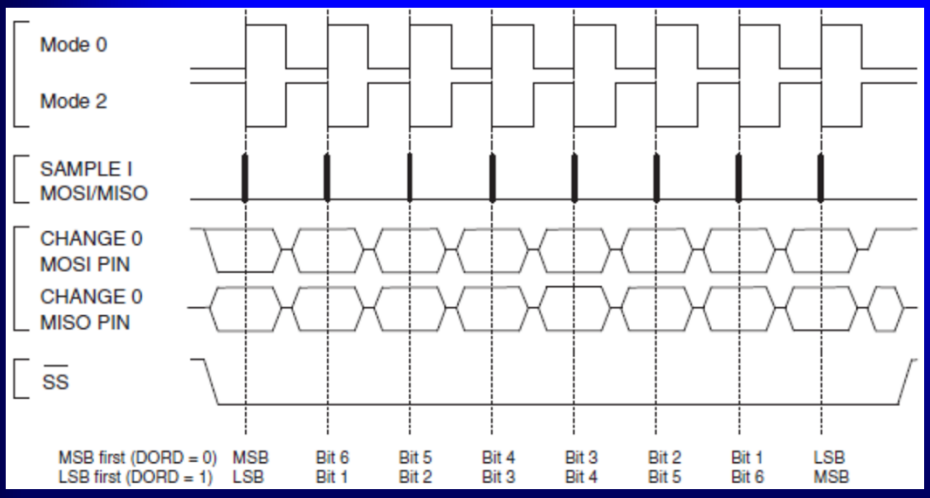
doc8331
Fig 22-2 (top)

## XMEGA: SPI Transfer Modes (CLK Phase/Polarity)




- See CTRL in section 22.7.1 and Table 22-2



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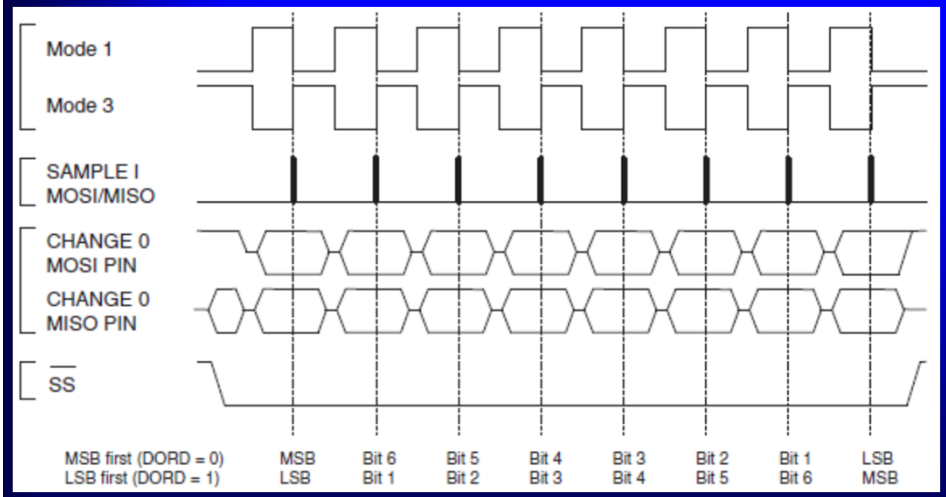
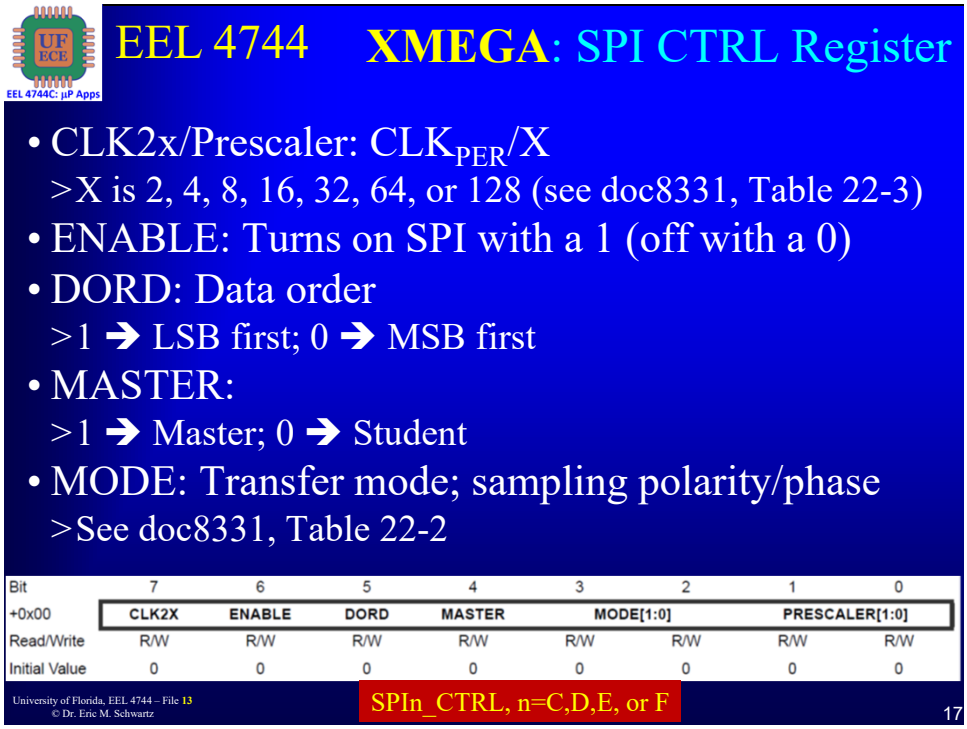
doc8331
Fig 22-2 (bottom)

## XMEGA: SPI Transfer Modes (CLK Phase/Polarity)




- See CTRL in section 22.7.1 and Table 22-2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XMEGA: SPI CTRL Register
• CLK2x/Prescaler: $CLK_{PER}/X$
>X is 2, 4, 8, 16, 32, 64, or 128 (see doc8331, Table 22-3)
• ENABLE: Turns on SPI with a 1 (off with a 0)
• DORD: Data order
>1 ➔ LSB first; 0 ➔ MSB first
• MASTER:
>1 ➔ Master; 0 ➔ Student
• MODE: Transfer mode; sampling polarity/phase
>See doc8331, Table 22-2
Bit 7 6 5 4 3 2 1 0
+0x00 CLK2X ENABLE DORD MASTER MODE[1:0] PRESCALER[1:0]
Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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SPIn_CTRL, n=C,D,E, or F
17

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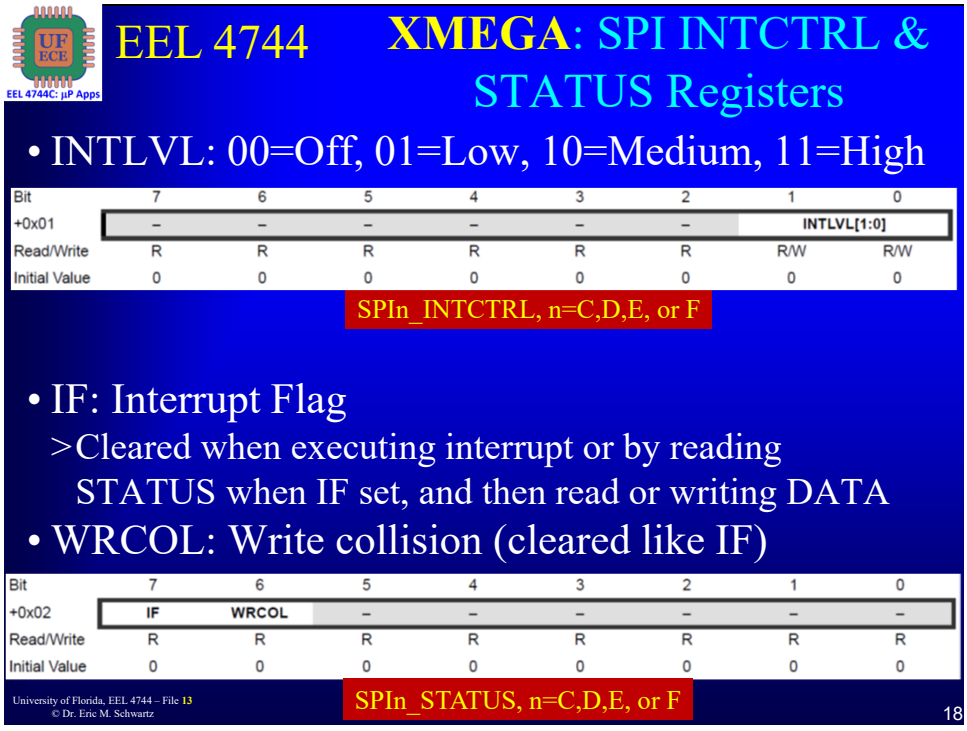
EEL 4744
XMEGA: SPI INTCTRL & STATUS Registers
• INTLVL: 00=Off, 01=Low, 10=Medium, 11=High
Bit 7 6 5 4 3 2 1 0
+0x01 – – – – – – INTLVL[1:0]
Read/Write R R R R R R R/W R/W
Initial Value 0 0 0 0 0 0 0 0
SPIn_INTCTRL, n=C,D,E, or F
• IF: Interrupt Flag
>Cleared when executing interrupt or by reading STATUS when IF set, and then read or writing DATA
• WRCOL: Write collision (cleared like IF)
Bit 7 6 5 4 3 2 1 0
+0x02 IF WRCOL – – – – – –
Read/Write R R R R R R R R
Initial Value 0 0 0 0 0 0 0 0
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SPIn_STATUS, n=C,D,E, or F
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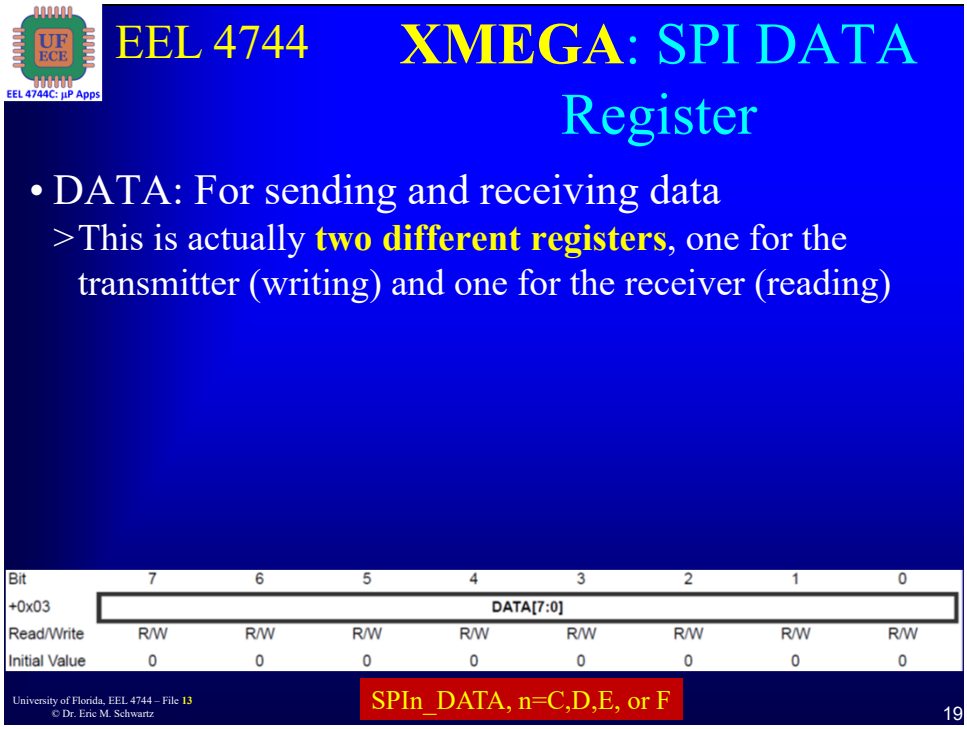
EEL 4744
XMEGA: SPI DATA Register
• DATA: For sending and receiving data
> This is actually two different registers, one for the transmitter (writing) and one for the receiver (reading)
Bit 7 6 5 4 3 2 1 0
+0x03 DATA[7:0]
Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
SPIn_DATA, n=C,D,E, or F
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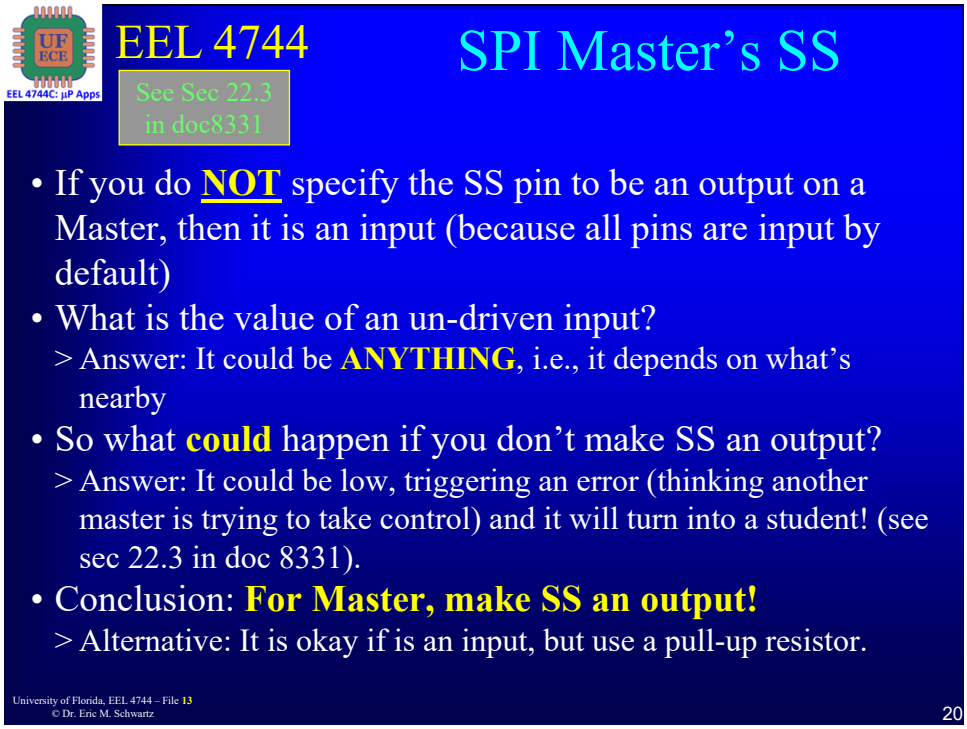
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See Sec 22.3 in doc8331
SPI Master's SS
• If you do NOT specify the SS pin to be an output on a Master, then it is an input (because all pins are input by default)
• What is the value of an un-driven input?
> Answer: It could be ANYTHING, i.e., it depends on what's nearby
• So what could happen if you don't make SS an output?
> Answer: It could be low, triggering an error (thinking another master is trying to take control) and it will turn into a student! (see sec 22.3 in doc 8331).
• Conclusion: For Master, make SS an output!
> Alternative: It is okay if is an input, but use a pull-up resistor.
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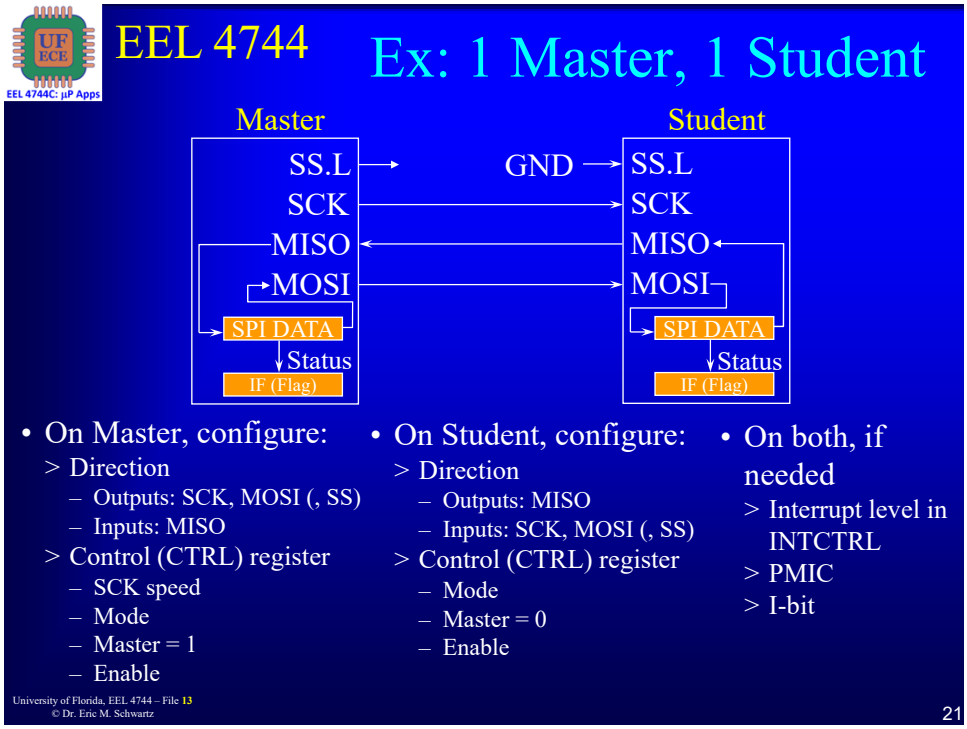
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Ex: 1 Master, 1 Student
Master
Student
SS.L
SCK
MISO
MOSI
GND
SPI DATA
Status
IF (Flag)
• On Master, configure:
> Direction
– Outputs: SCK, MOSI (, SS)
– Inputs: MISO
> Control (CTRL) register
– SCK speed
– Mode
– Master = 1
– Enable
• On Student, configure:
> Direction
– Outputs: MISO
– Inputs: SCK, MOSI (, SS)
> Control (CTRL) register
– Mode
– Master = 0
– Enable
• On both, if needed
> Interrupt level in INTCTRL
> PMIC
> I-bit
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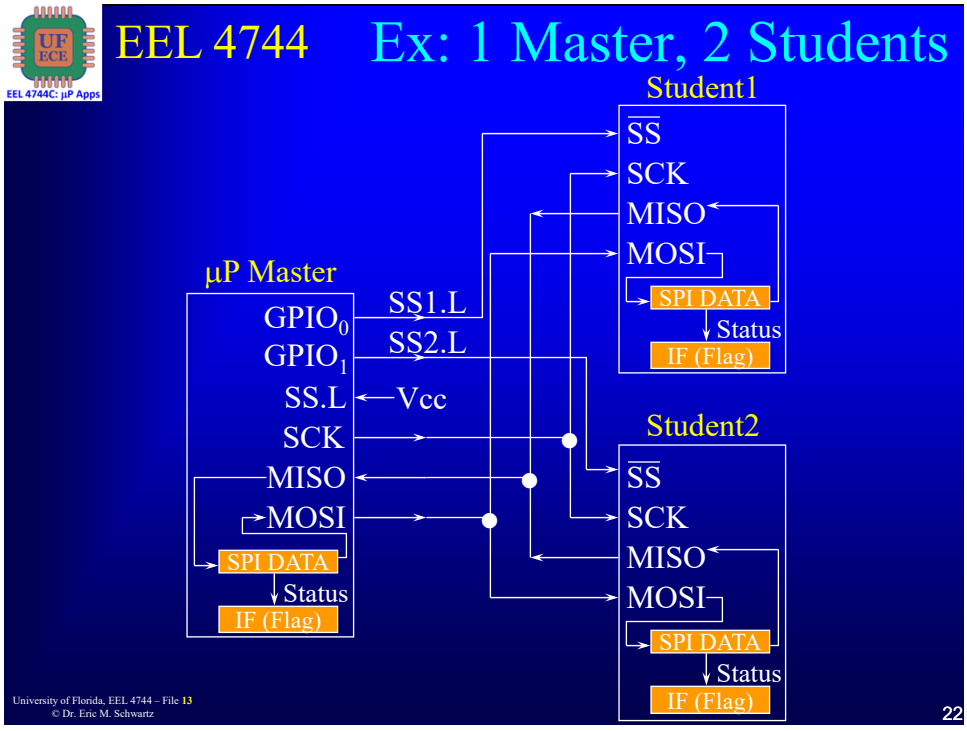
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Ex: 1 Master, 2 Students
Student1
Student2
µP Master
SS
SCK
MISO
MOSI
GPIO0
GPIO1
SS1.L
SS2.L
SS.L
Vcc
SPI DATA
Status
IF (Flag)
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## SPI Concepts

- **I/O Serial Ports** - Microcontroller Expansion
- The most limited resource of a microcontroller is the number of I/O lines (pins) available
- The SPI and shift registers can expand the I/O capabilities with only 3 pins (MISO, MOSI, SCK)
- A write to the SPI transfers serially 8 bits with 8 clock pulses
- Shift registers receive the serial data and convert it to parallel for I/O processing



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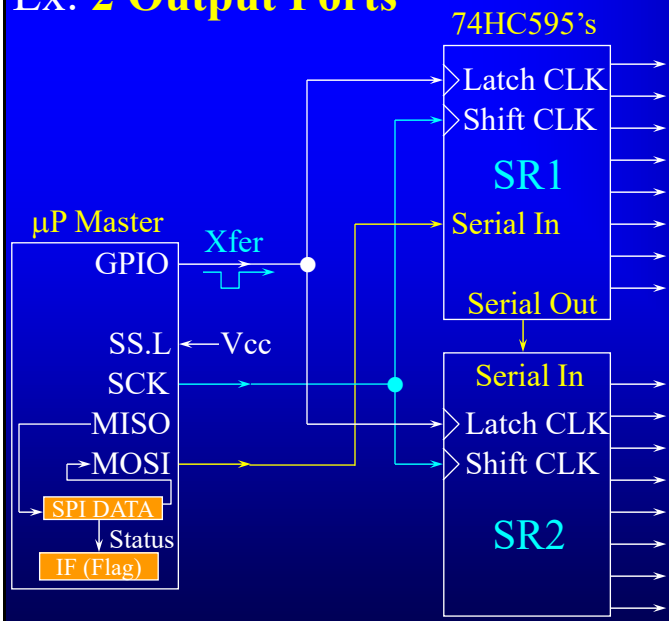
## Ex: 2 Output Ports




**How to Program**

- Make GPIO high (1)
- Calculate the 2 bytes for output
- Send SR2's byte to the SPI DATA
  - 8-bits shift into SR2
- Send SR1's byte to the SPI DATA
  - 8-bits shift into SR1
- Send 0 then 1 (low pulse) to GPIO
  - Parallel pins updated on the rising edge of low pulse
- 16 output bits are now in place, but parallel I/O pins are unaffected



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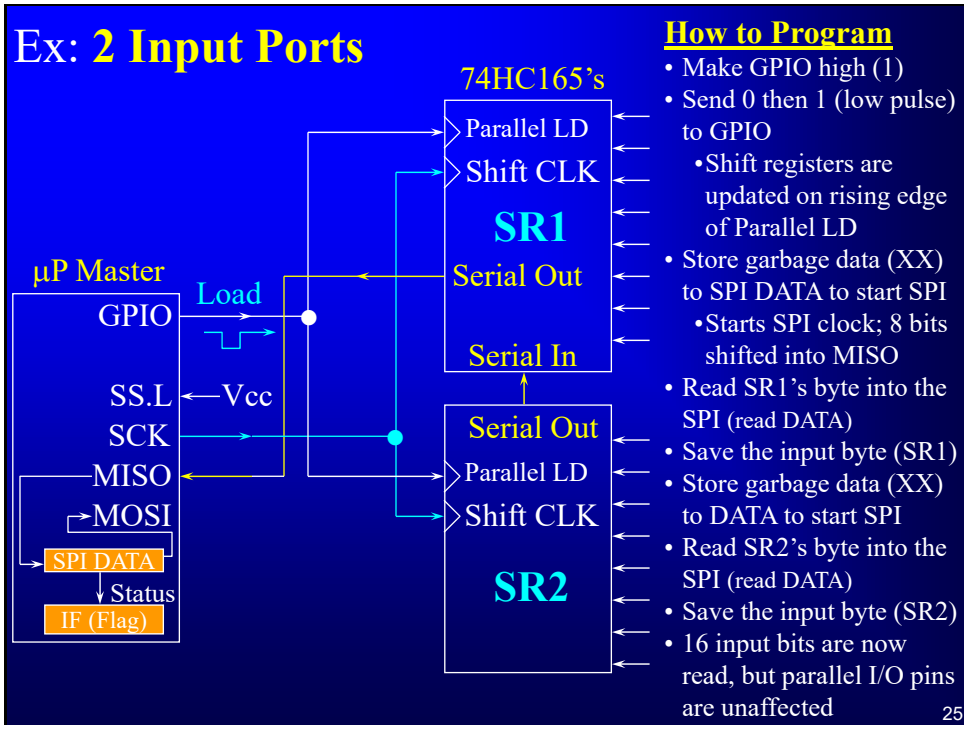


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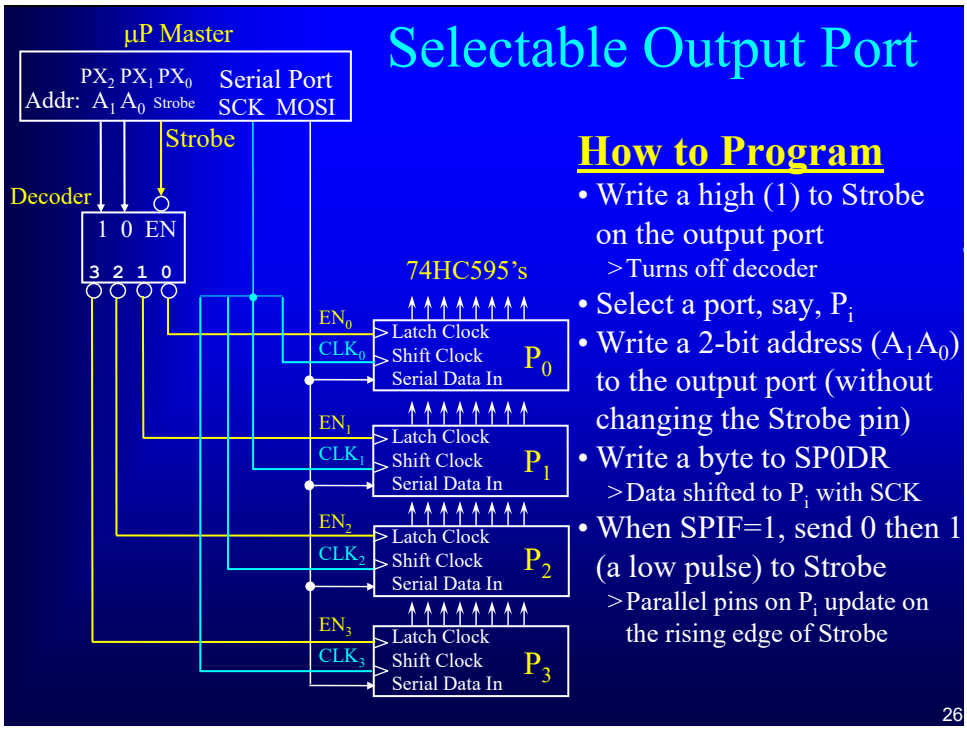


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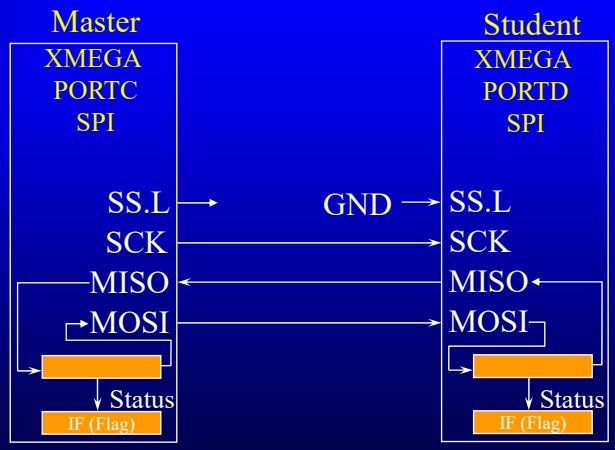
## SPI Examples (Live)
## Ex: 1 Master, 1 Student

- I'll show some live examples with the below setup.



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## SPI Examples (Live)
## Ex: 1 Master, 1 Student

- Open the following:
  > doc8331, section 22; doc8385, section 33.2
  > Include file from Microchip Studio
- Ex1: Setup a master to transmit a single byte and receive a single byte from a student; *SPI_M_SWAP_BYTE.asm*
- Ex2: Setup a student to transmit a single byte and receive a single byte from a master; *SPI_S_SWAP_BYTE.asm*
- Ex3: Setup a master **AND** student to exchange a byte; *SPI_M_S_SWAP_BYTE.asm*
- Ex4: Setup a master to transmit a table of bytes and receive a table of bytes from a student; *SPI_M_SWAP_BYTES.asm*
- Ex5: Setup a student to transmit a table of bytes and receive a table of bytes from a master; *SPI_S_SWAP_BYTES.asm*

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# IPPD and "Turtle Tracker"

- IPPD = Integrated Product & Process Design
  - > A two semester capstone design course for engineers
- MATR: Marine Animal TrackeR
  - > Attaching to turtle
  - > Sensors
  - > Satellite connection
  - > Data processing



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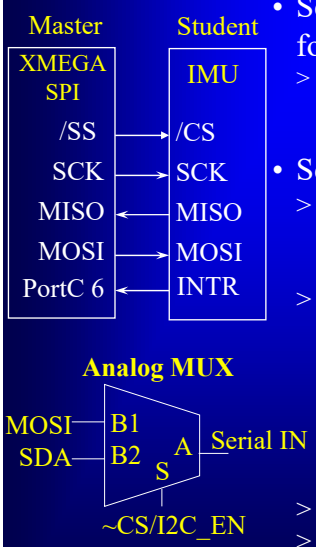
# Lab 6: Interfacing w/ IMU




- See Robotics backpack analog (MUXes) switches for IMU using SPI or I2C (**below left**)
  - > MUX is used to selects which (SPI or I2C) signals are used for IMU (if S is low, SPI used; if S is high I2C); see OOTB Robotics Backpack schematic; (similar for SCK for SPI is Serial CLK)
- See IMU document
  - > See Fig 3 (in either LSM6DSL or LSM6DS3TR); compare to XMEGA SPI timing
    - – CS (chip select), SPC (SPI clock), SDI/SD0 (data input/output)
  - > Read § 6.4 in LSM6DSL [§ 6.2 in LSM6DS3TR] - SPI bus interface
    - – LSM6DSL Fig 9 [8]; compare to XMEGA SPI timing
      - In Fig 9, R/~W is the first bit in the address, telling you if reading or writing to the IMU
        - SDI (input to IMU): R /W ADR6:ADR0 | DI7:DI0
        - SDO (output from IMU): X7:X0 | DO7:DO0 (X not used)
  - > Table 6: SPI clock frequency maximum
  - > Section 8 – Register mapping
    - – WHO_AM_I (Read only, at address 0x0F)
      - Value is 0x6A [0x69], for LSM6DSL[for LSMDS3TR]



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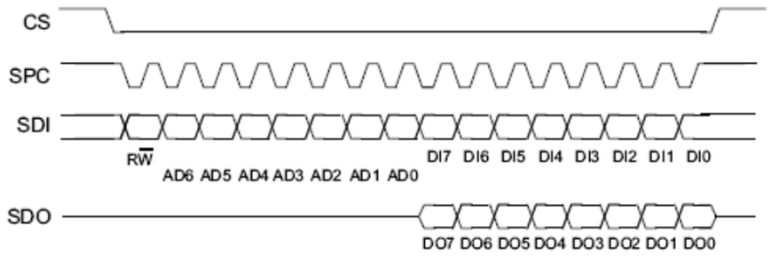
# More IMU Info

- Write requires two SPI transmissions
  - > First with R/~W first bit low for write and the next 7 bits the register address that you want to write to
  - > For the second, write the data you want to send to that register
- For a read, it also requires two bytes
  - > First send a byte with the first bit low for a read and then supply the register; the next 7 bits are the configuration register address that you want to read.
  - > Then just send garbage; while the garbage is coming in, the µP will read the 8-bit data from the previously selected IMU configuration register.




LSM6DSL Fig 9 (LSM6D3TR Fig 8)

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# More IMU Info

**CTRL3_C**
LSM6DSL § 9.15
LSM6D3TR § 9.14

- Under Figure 9 (or 8): "In multiple read/write commands further blocks of 8 clock periods will be added. When the CTRL3_C (12h) (IF_INC) bit is '0', the address used to read/write data remains the same for every block. When the CTRL3_C (12h) (IF_INC) bit is '1', the address used to read/write data is increased at every block."
- OUTX_H | OUTX_L (and similar for Y and Z) for 16-bit 2's complement acceleration values (high byte | low byte).



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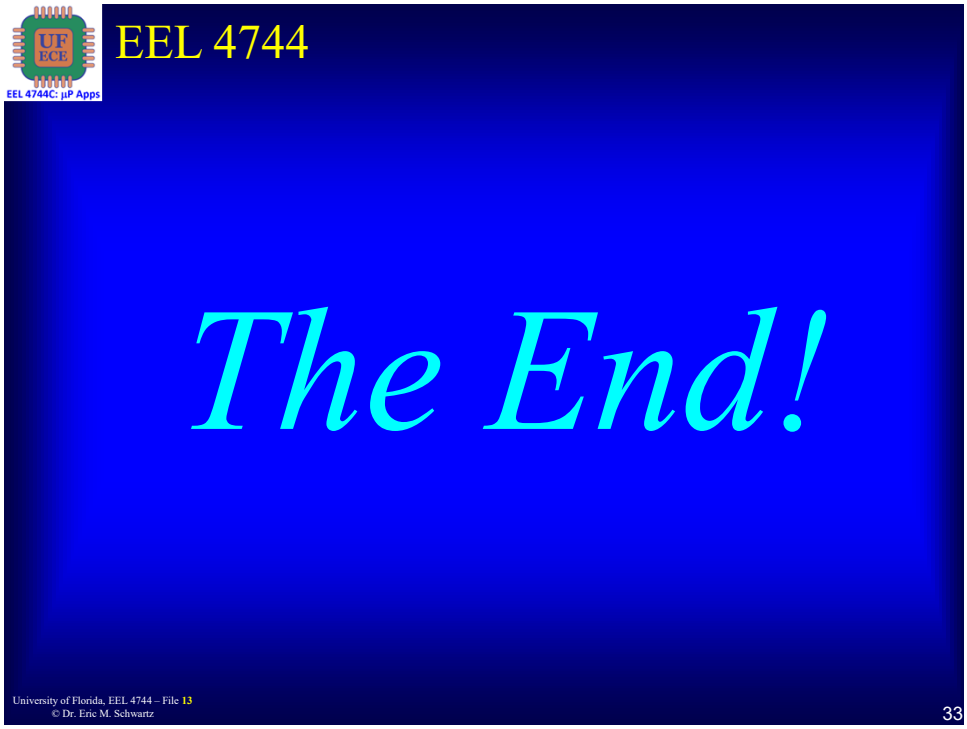
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EEL 4744C: µP Apps
The End!
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